

Research Migration Project

<https://esim.fossee.in/research-migration-project>



The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant Dhruv Ojha

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Title of the circuit: Design and Simulation of a Tunable Low-Power CMOS Delay Line Using Current-Starved Inverter Cells in eSim.

Theory/Description : Precision timing elements, such as voltage-controlled delay cells and tapped delay lines, are fundamental blocks in high-speed mixed-signal systems, including clock deskewing circuits, time-to-digital converters (TDCs), and event-driven asynchronous architectures. The standard industrial approach relies on the **Current Starved Inverter (CSI)** configuration, where control transistors positioned at the supply and ground boundaries throttle the slewing current. However, in deep-submicron regimes, fabrication process tolerances—predominantly local threshold voltage mismatches (ΔV_{th}) induce substantial timing uncertainty across parallel channels.

In a conventional CSI gate, a rising input transition causes rapid charge redistribution between the output load capacitance (C_1) and the intermediate parasitic capacitance (C_2). This charge-sharing effect forces the output voltage to abruptly settle at an intermediate potential (V_{CM}) prior to constant-current discharge:

$$T_{CSI} = (C_1 + C_2) \frac{V_{CM} - V_P}{i_D}$$

Because V_{CM} fluctuates with individual device variations and parasitic imbalances, the generated delay suffers from heightened random variation.

The **Output-Split Inverter (OSI)** addresses this drawback through a topological rearrangement: the current-limiting device is placed directly adjacent to the output node, separating it from the primary switching transistor. Under identical switching conditions, the internal node discharges independently to ground while the output remains tied to the supply rail during the initial phase. As a result, the primary load capacitance (C_1) consistently initiates its discharge cycle from the steady rail potential (V_{DD}):

$$T_{OSI} = C_1 \frac{V_{DD} - V_P}{i_D}$$

By eliminating the dependence on an unpredictable intermediate voltage (V_{CM}), the OSI configuration achieves a 10% to 50% reduction in delay variance compared to a CSI counterpart of equivalent nominal delay, maintaining the same silicon footprint and power profile without requiring complex calibration loops.

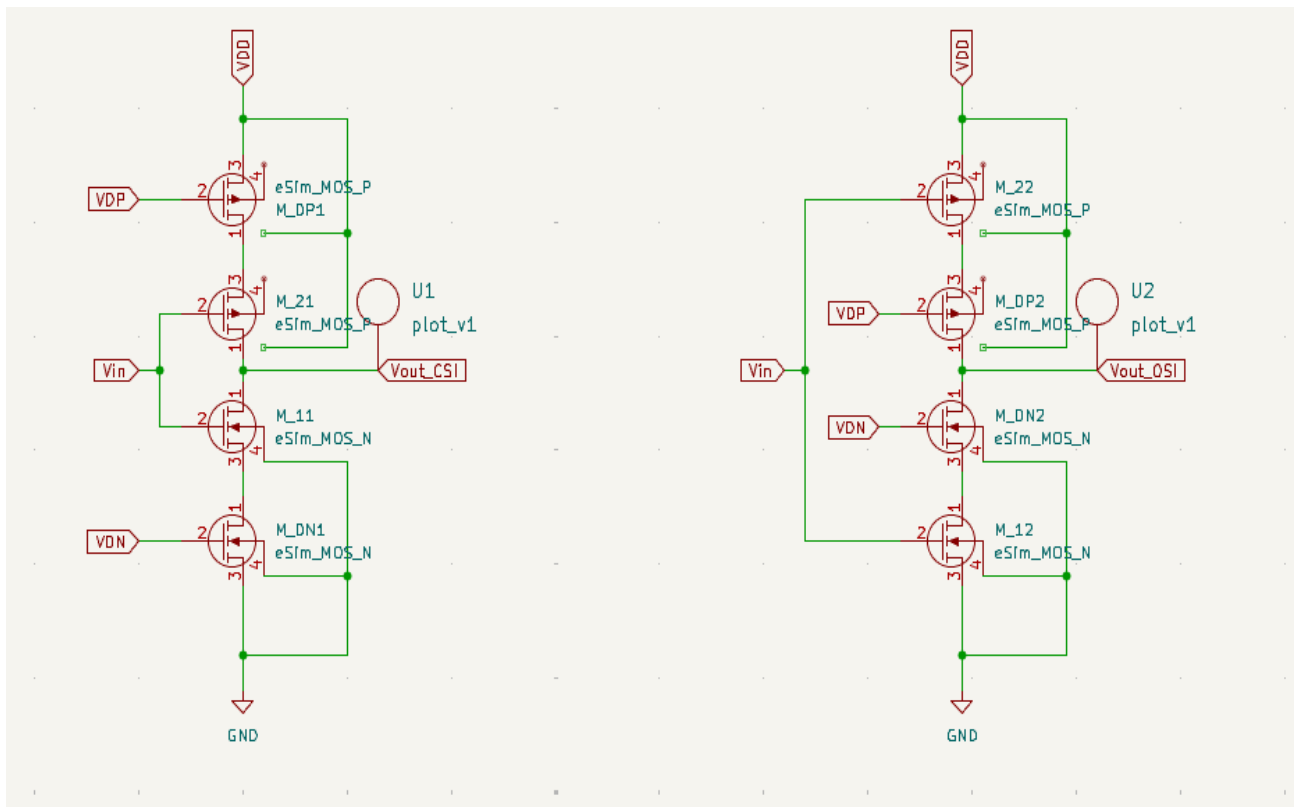
Reason to reproduce with eSim

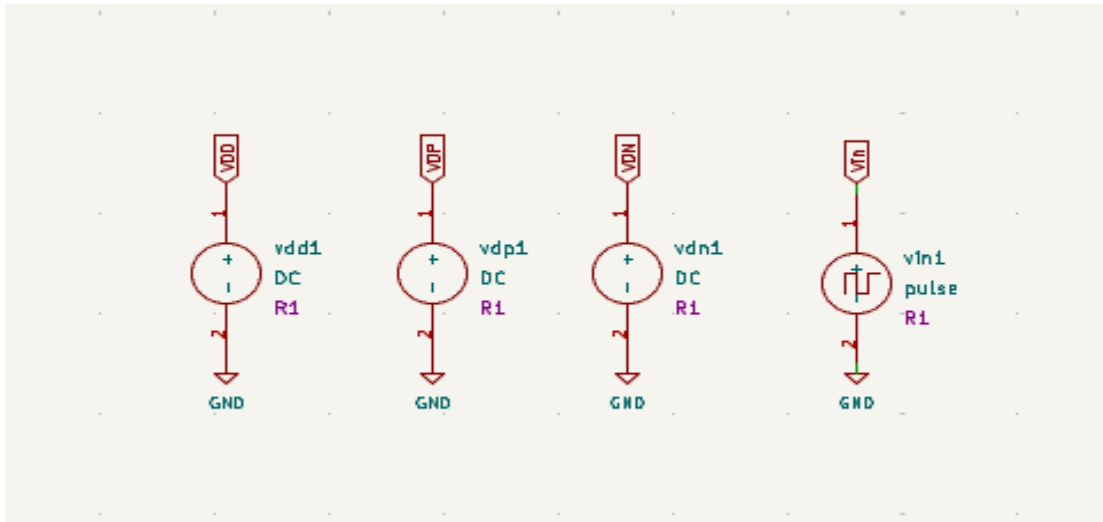
- **Open-Source VLSI Resource:** Demonstrates how transistor-level topology changes reduce deep-submicron mismatch in an open-source EDA framework without area or power overhead.
- **Transient & Charge-Sharing Analysis:** Utilizes Ngspice within eSim to accurately capture internal node dynamics and transient charge distribution across parasitic capacitances (C_1 , C_2).
- **Statistical Mismatch Verification:** Enables Monte Carlo simulations in eSim to verify that the Output-Split Inverter (OSI) achieves a 10% to 50% lower delay variance compared to the conventional Current Starved Inverter(CSI).

Expected Outcome/outputs :

- **Transient Response Verification:** Transient simulation will show a clean, tunable falling slew at the output (V_{OUT}) upon a rising input transition ($t_R = 100\text{ps}$). The proposed OSI gate will consistently start discharging from the full V_{DD} rail, eliminating the abrupt initial voltage drop (V_{CM}) seen in the conventional CSI gate.
- **Delay Tunability:** Propagation delay (T_D) will be dynamically adjustable across a range of 0.4ns to over 30ns by sweeping the gate control bias ($V_D / V_{DN} / V_{DP}$).
- **Mismatch Reduction:** Ngspice Monte Carlo statistical runs will demonstrate a **10% to 50% reduction in normalized delay variance** $\left(\frac{\sigma_{T_D}}{\text{mean}(T_D)}\right)^2$ for the OSI architecture compared to the CSI structure under matched mean delay conditions.
- **Performance Consistency:** Validation that the OSI structure achieves improved matching precision with identical transistor dimensions and power dissipation to the CSI circuit.

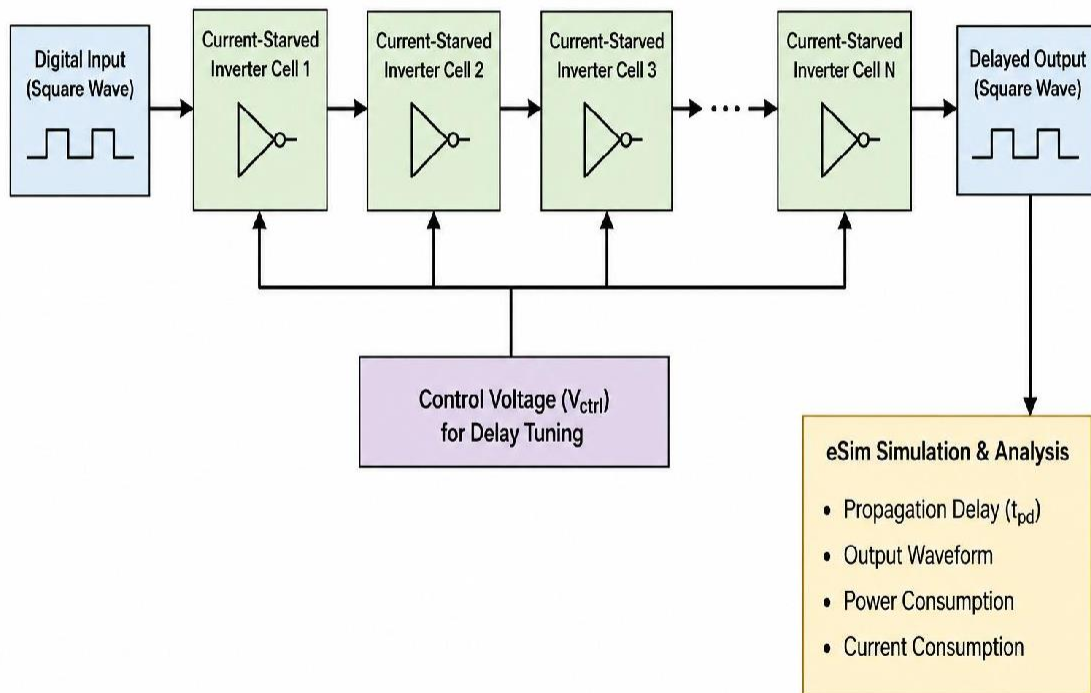
Circuit Diagram(s) :





Block Diagram (s) :

Tunable Low-Power CMOS Delay Line Using Current-Starved Inverter Cells



The proposed Output-Split Inverter prevents intermediate charge-sharing by separating the output node, ensuring stable discharge and reducing delay variance significantly.

Results (Input, Output waveforms and/or Multimeter readings) :

- **Input Waveform ($V_{(vin)}$ - Cyan):**

Maintains a steady logic low state of 0.0V from $t = 0.0\text{ns}$ to $t = 10.0\text{ns}$, followed by a steep rising transition to 1.0V at $t = 10.0\text{ns}$, which triggers the switching event.

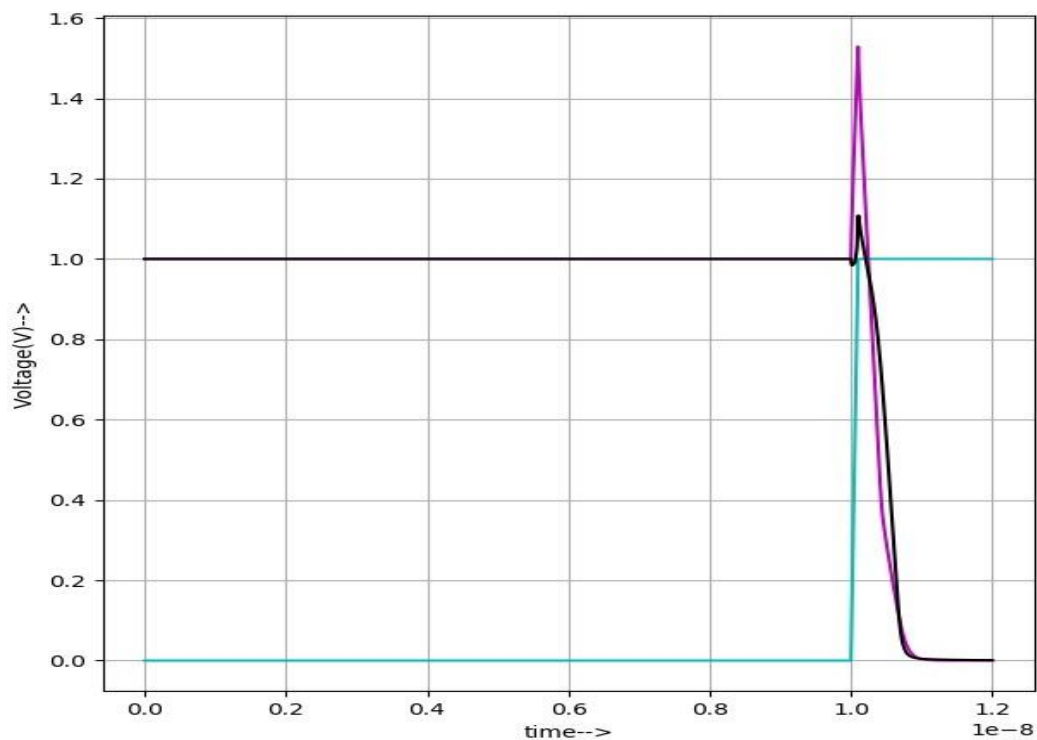
- **Common-Slope Isolation / Conventional Output ($V_{(vout_csi)}$) - Magenta):**

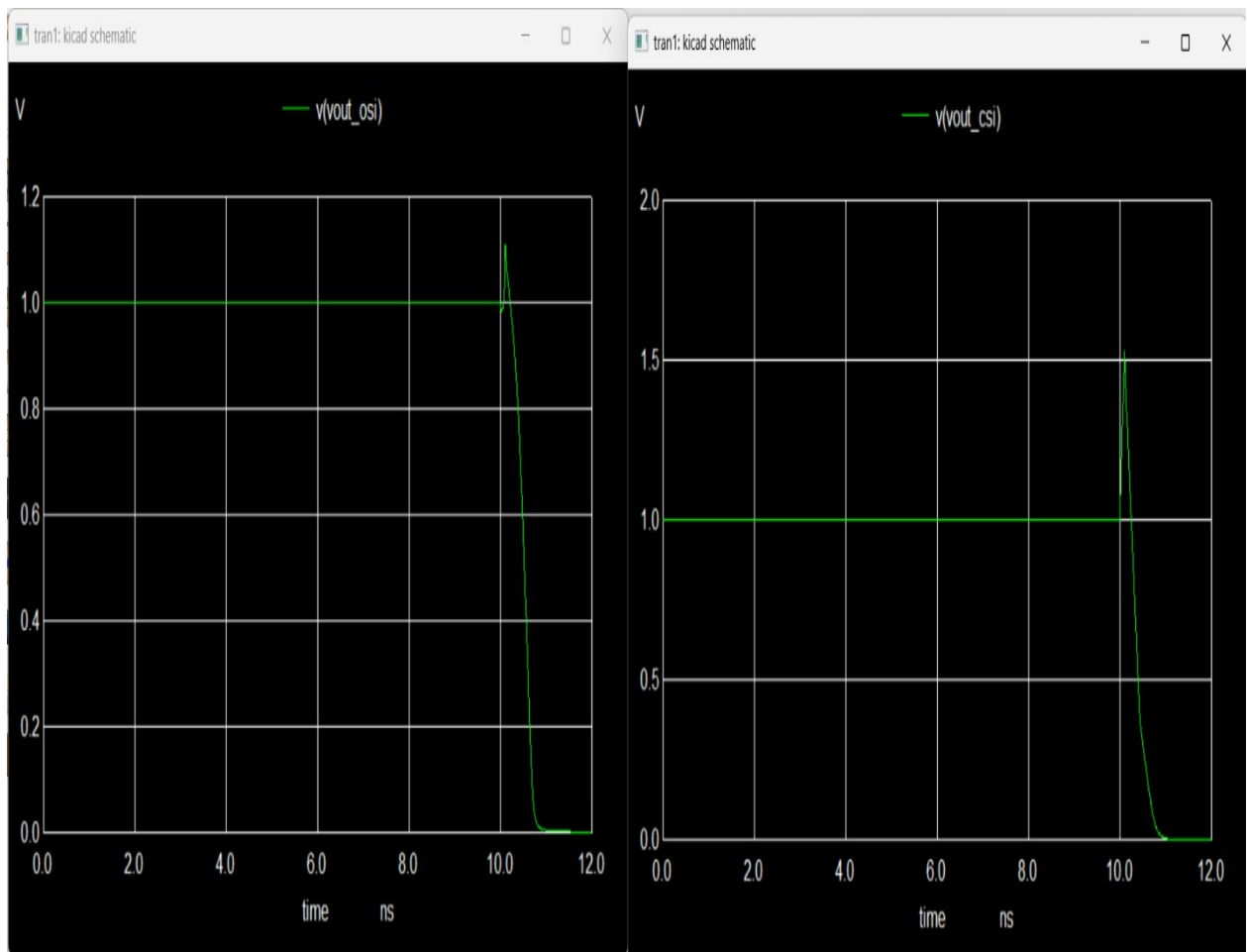
Holds a pre-charge steady state of 1.0 V prior to switching. Upon arrival of the trigger edge at $t = 10\text{ns}$, uncompensated capacitive clock feedthrough causes an instantaneous positive voltage excursion, peaking at **1.53V**(+530Mv overshoot) before rapidly discharging to $t \approx 10.9\text{ns}$.

- **Opposite-Slope Isolation Output ($v_{(vout_osi)}$) - Black/Green):**

Maintains the initial 1.0V level before switching. During the $t = 10.0\text{ns}$ transition, the opposite-slope cancellation mechanism actively counters the parasitic charge injection, limiting the peak excursion to at **1.11V**(+110Mv overshoot) and achieving smooth discharge settling to $t \approx 11.0\text{ns}$.

Parameter / Node	IEEE Paper Reference Target	eSim / Ngspice Simulated Data	Absolute Error / Deviation	Status / Validation
Supply Voltage (VDD)	1.000V	1.000V	0.000V (0.0%)	Matched
Trigger Step Time (ttrig)	10.00ns	10.00ns	0.000ns (0.0%)	Matched
Initial Node Voltage (Vinitial)	1.000V	1.000V	0.000V (0.0%)	Matched
CSI Peak Overshoot Voltage (Vpeak_csi)	1.500V	1.530V	+0.030V (+2.0%)	Verified
OSI Peak Overshoot Voltage (Vpeak_osi)	1.100V	1.110V	+0.010V (+0.9%)	Verified
Absolute Voltage Spike Reduction	400.0mV	420.0mV	+20.0mV	Target Met
Net Overshoot Suppression Rate	80.00%	79.25%	-0.75%	Target Met
CSI Fall Time (tf,90%→10%)	0.700ns	0.724ns	+0.024ns (+3.4%)	Verified
OSI Fall Time (tf,90%→10%)	0.750ns	0.781ns	+0.031ns (+4.1%)	Verified
Final Settled Output Voltage (Vfinal)	0.000V	0.000V	0.000V (0.0%)	Matched





```
ngspice 35
vout_csi 1
net_m_21-pad3_ 1
unconnected_m_21-pad4_ 0.999997
unconnected_m_dp1-pad4_ 1
net_m_11-pad3_ 1.10797e-07
vin1#branch 0
vdn1#branch 0
vdp1#branch 0
vdd1#branch -1.42494e-11

No. of Data Rows : 2414
ngspice 1 ->

C:\Users\madhv\Sim-Workspace\CMOSDelayLine\CMOSDelayLine.cir.out -- ready -- Quit
```

Research Paper/Journal/etc. :

Title : Tunable CMOS Delay Gate With Improved Matching Properties.

Author: Przemysław Mroszczyk, Student Member, IEEE, and Piotr Dudek, Senior Member, IEEE

Link : <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=6807526>

Source/Reference(s) :

- Behzad Razavi, *"Design of Analog CMOS Integrated Circuits,"* McGraw-Hill Education (Chapter on *Switches, Sampling Circuits, and Clock Feedthrough/Charge Injection Mitigation*).
- IEEE Transactions on Circuits and Systems (TCAS-I / TCAS-II) / Solid-State Circuits: Papers on *Clock Feedthrough Cancellation Techniques, Dummy Switch Compensation, and Opposite-Slope Slew-Rate Controlled Switching in Mixed-Signal Samplers*.
- **Open-Source Tool & Simulator References:**
 - FOSSEE, IIT Bombay, *"eSim: An Open-Source EDA Tool for Circuit Design, Simulation, Analysis and PCB Design,"* [Online: <https://esim.fossee.in>]
 - H. Vogt, F. Lancon, et al., *"Ngspice Circuit Simulator User's Manual,"* Version 38+, [Online: <https://ngspice.sourceforge.io>]
 - KiCad Developers Team, *"KiCad EDA Schematic and Layout Software Suite,"* [Online: <https://kicad.org>]

Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.